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Abstract
Programmable logic arrays (PLAs) are widely used for realizing arbitrarycombinational and sequential logic function in VLSI systems
because of its design simplicity, structural regularity, and predictable performance.Recently, microprocessors use Dynamic Programmable Logic Array (DPLAs) to implement such functions as instruction decoding. Due to the regularity in structure, many previous researches have devoted to the analysis of developing high speed or low power DPLAs by adding some logic gates or amending the internal buffer.
Unfortunately, design automation for DPLAs becomes more difficult due to the existance of these components.Also the circuit functionality may dominate the structures been chosen.In this paper, we have proposed a new low power PLA scheme by employing logic minimization and structure reorganization to further reduce the power consumption and ease of design automation.On the other hand, we have improved the Wang's DPLA design to overcome the race condition in the OR plane. Based on these two DPLA schemes, we have implemented a set of cell library that can be used in the design automation for DPLA compiler.
The cell library includes the basic transistors in the AND/OR plane, the Input/Output buffers, inter-buffers, and one clock buffer.
Given a personality of a PLA function and the predesigned cells, our DPLA compiler starts from the logic minimization and followed by the reconstruction. Critical path identification and timing analysis is then proceeded and a better scheme will be chosen for the main structure to be synthesized.
From the experimental results, we can find that our DPLA compiler can generate the specific layout diagram and SPICE netlist with respect to each different MCNC benchmark circuit.All the physical verification (DRC/LVS) of these circuits are proven to be correct. Besides, the performance of synthesized circuits can operate beyond 250MHz.
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